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ABSTRACT OF THE DISCLOSURE

A remodulator system includes a source of an input transport packet stream and an input packet buffer coupled to the input transport packet stream

5   source. The input packet buffer generates a status signal indicating whether it is: full, empty, or neither empty nor full. An output packet stream generator is coupled to the input packet stream buffer and responsive to an output clock signal, and generates the output packet stream in synchronism with the output clock signal. A variable output clock signal generator generates the output clock

10 signal responsive to a control signal, and a control signal generator generates the control signal in response to the status signal.